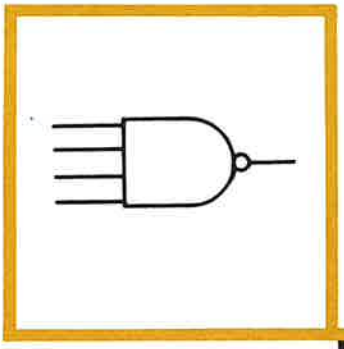
91-050
May 1965
New information



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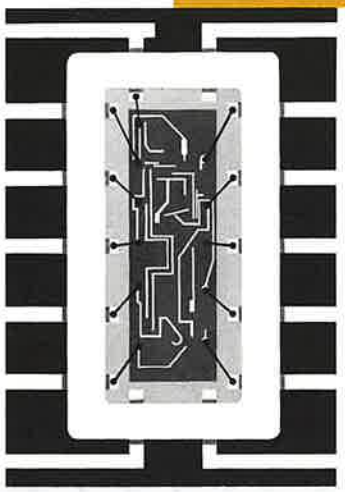
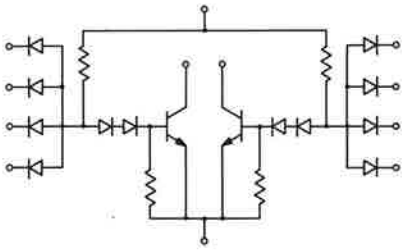
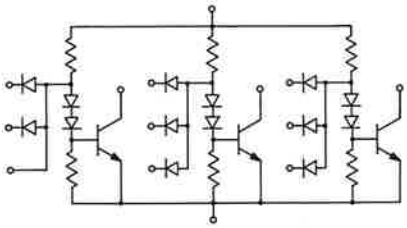


industrial-commercial integrated circuits

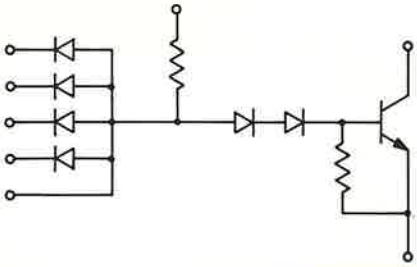
WC 211 G,T Dual NAND Gate
4 input



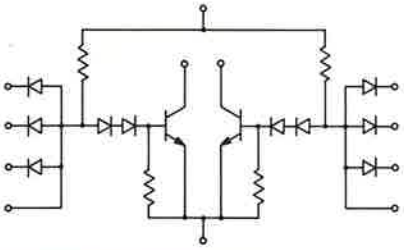
WC 206 G Triple NAND Gate
Two 3 inputs; one 2 input with node



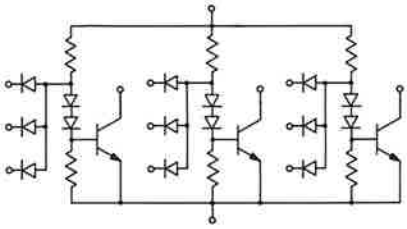
WC 204 G,T Single NAND Gate
4 input with node



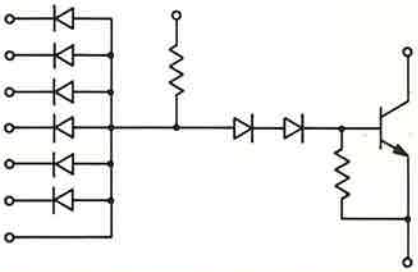
WC 221 G,T Dual NAND Gate
3 input with nodes



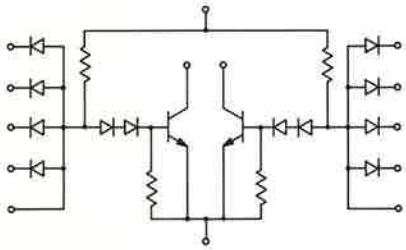
WC 216 G Triple NAND Gate
Three 3 inputs



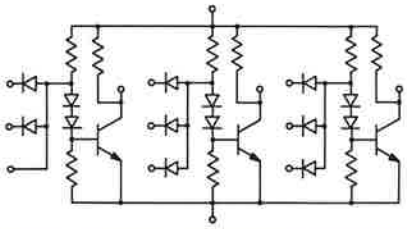
WC 214 G,T Single NAND Gate
6 input with node



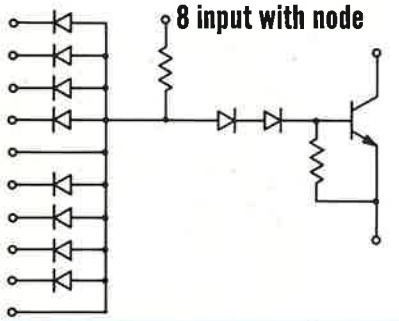
WC 231 G Dual NAND Gate
4 input with nodes



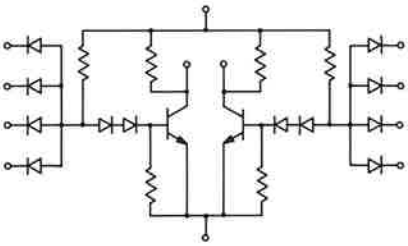
WC 226 G Triple NAND Gate
Two 3 inputs, one 2 input
with node, collector resistors



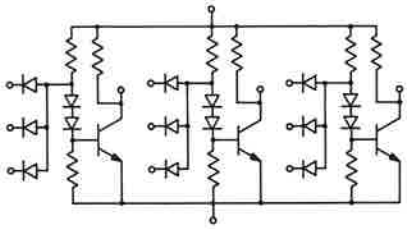
WC 224 G,T Single NAND Gate
8 input with node



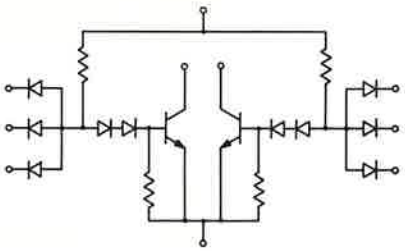
WC 241 G Dual NAND Gate
4 input with collector resistors



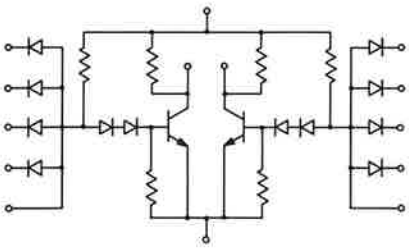
WC 236 G Triple NAND Gate
Three 3 inputs, collector resistors



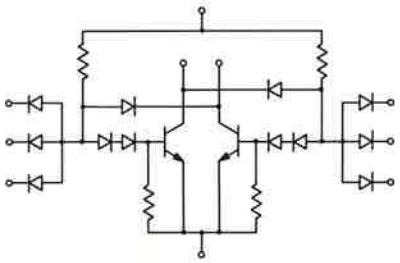
WC 201 G,T Dual NAND Gate
3 input



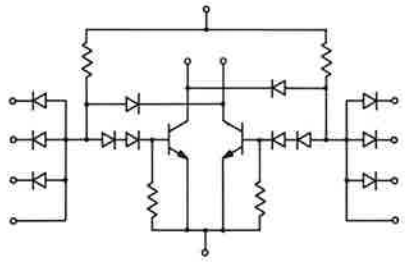
WC 261 G Dual NAND Gate
4 input with nodes, collector resistors



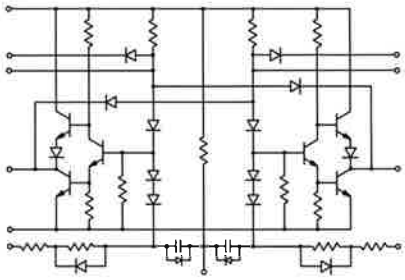
WC 202 G,T
RS flip flop 3 input



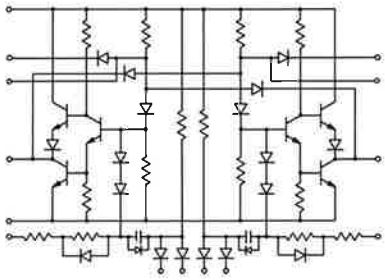
WC 212 G,T RS flip flop
3 input with nodes



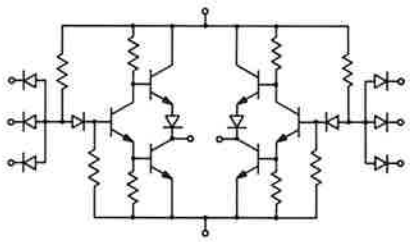
WC 213 G,T pulse binary counter



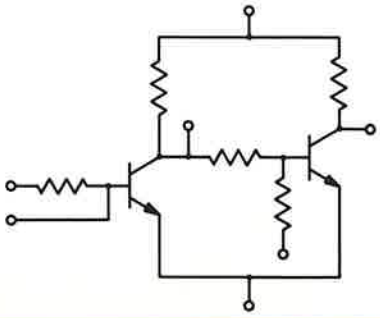
WC 215 G,T JK flip flop



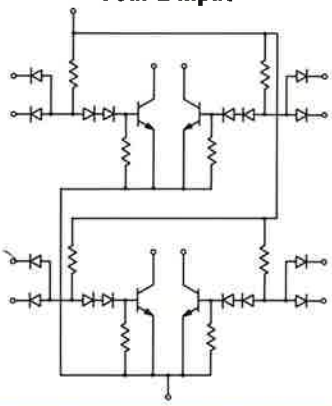
WC 210 G,T line driver
Two 3 input



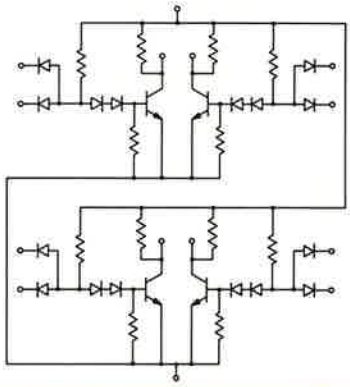
WC 208 G,T Level Detector-Schmitt Trigger



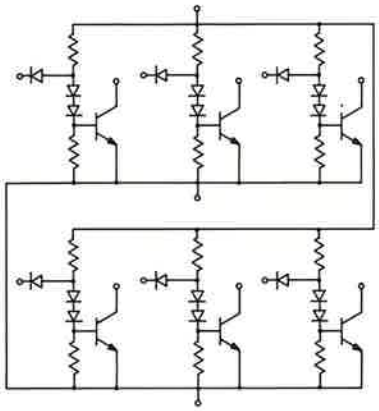
WC 246 G Quad NAND Gate
Four 2 input



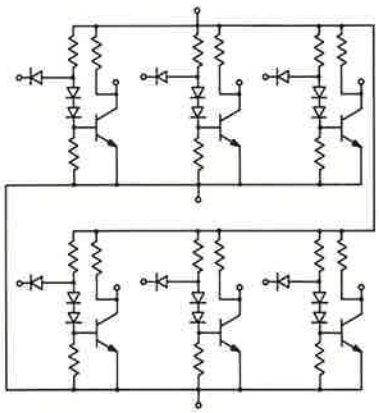
WC 266 G Quad NAND Gate
Four 2 input; collector resistors



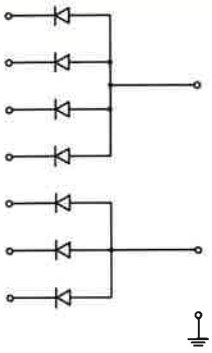
WC 286 G Hex NAND Gate
Six 1 input



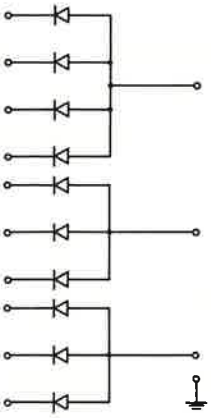
WC 296 G Hex NAND Gate
Six 1 input; collector resistors



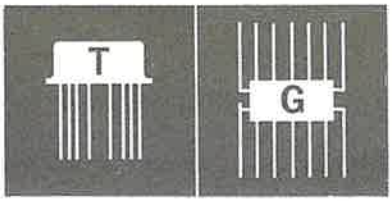
WC 217 G,T
diode array



WC 227 G,T diode array



packages



8 or 12 lead
TO-5 pack

14 lead ¼" x ⅛"
FLAT-PAK™

Electrical Characteristics

parameter	symbol	values at temperature: limit	+25°C	0° to 75°C worst case	units
STANDARD GATE CHARACTERISTICS (FOR V_{cc}=6.0 VOLTS)					
power consumption, per gate, 50% duty cycle	P_c	max. typ.	9.5 7.5	10.5	mw mw
input current, input grounded	I_{in}	max.	1.80	2.10	ma
input voltage for 0-state output, fan-out of six	$V_{in}/0$	min.	1.80	2.10	volts
input voltage for 1-state output, fan-out of one	$V_{in}/1$	max.	1.00	0.60	volts
output current @ specified $V_{CE(SAT)}$	I_{out} $V_{CE(SAT)}$	min. typ. max.	20 32 0.45		ma ma volts
fan-out available each gate	F_o	min.	11	6	...
noise margin, worst case	ΔV_n	typ. min.	1.00 0.55	0.25	volts
average switching time $(T_{on} + T_{off}) \div 2$	T_{avs}	typ. max.	23 32	23	ns
ring propagation delay time, (ring of five gates)	T_{rpd}	typ.	30	30	ns
SPECIAL CHARACTERISTICS (FOR V_{cc}=6.0 VOLTS)					
WC 213 power consumption, total	P_c	max. typ.	50 35	52 39	mw mw
fan-out available each output @ standard $V_{CE(SAT)}$	F_o	min.	9	7	...
count rate	f_c	min. typ.	10 12	8 10	mc mc
WC 215 power consumption, total	P_c	max. typ.	56 45	65 52	mw mw
fan-out available each output @ standard $V_{CE(SAT)}$	F_o	min.	9	7	...
count rate	f_c	typ.	5	4	mc
WC 210 power consumption, total, 50% duty cycle	P_c	max.	33	36	mw
input current, input grounded	I_{in}	max.	1.80	2.10	ma
output current @ $V_{CE(SAT)}$ = 0.60 volts	I_{out}	min.	40	30	ma
fan-out available each output @ standard $V_{CE(SAT)}$ and I_{in}	F_o	min.	17	12	...
average switching time $(T_{on} + T_{off}) \div 2$	T_{avs}	max. typ.	75 53	100 71	ns ns
ring propagation delay time, (ring of five drivers)	T_{rpd}	typ.	45	52	ns

All values shown subject to design change for product improvement.

Features

- Fan-out 11 minimum
- Noise margin typically greater than 1 volt—guaranteed minimum 550 mv
- 19 ns average switching time
- 9.5 mw maximum power consumption per gate
- Single 6 volt power supply required
- 0° to +75°C temperature range
- AND-OR-NOT function in one stage
- Compatible driver: fan-out 17 minimum; drives 40 ma, 250 pf
- Compatible binary counter and shift register elements; dc and ac coupled; counting rates to 12 mc
- Expandable fan-in through diode arrays
- 14 lead ¼" x ⅛" G style FLAT-PAK™ makes possible increased logic power per package

Westinghouse Electric Corporation

MOLECULAR ELECTRONICS DIVISION

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